

### **QDD-400GB-VSR4-DE-C**

Dell® Compatible TAA 400GBase-SR4 PAM4 112G QSFP-DD Transceiver (MMF, 850nm, 50m, MPO-12, DOM, CMIS 4.0)

#### **Features:**

- 53.125 GBd PAM4 4 channel 400G-SR4 Optical interface
- 26.5625 GBd PAM4 8 channel 400G AUI-8 C2M Electrical interface
- Compliant with IEEE 802.3ck and IEEE 802.3db
- QSFP-DD MSA package with MPO-12 APC
- Multi-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- CMIS Rev4.0
- RoHS Compliant and Lead Free



#### **Applications:**

- 400GBase Ethernet
- Datacenter switch

#### **Product Description**

This Dell® QSFP-DD transceiver provides 400GBase-SR4 throughput up to 50m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO-12 connector. It is guaranteed to be 100% compatible with the equivalent Dell® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	V <sub>cc</sub>	3.1	3.3	3.5	V	
Storage Temperature	T <sub>stg</sub>	-40		85	°C	
Operating Case Temperature	T <sub>c</sub>	0		70	°C	
Operating Relative Humidity	RH	5		85	%	1
Optical Input Power	P <sub>IN</sub>			5	dBm	

### Notes:

1. Non-condensing.

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Supply Voltage	V <sub>CC</sub>	3.135	3.3	3.465	V	
Supply Current	I <sub>CC</sub>			2640	mA	
Module Power Dissipation	P			8	W	
Transmitter						
Differential Input Impedance	Z <sub>IN</sub>		100		Ω	
Receiver						
Differential output Impedance	Z <sub>os</sub>	90	100	110	Ω	
Common-Mode to Differential-Mode Return Loss	RL <sub>dc</sub>	Note 1			dB	
Transition Time, 20 to 80%	T <sub>r</sub> , T <sub>f</sub>	8.5			ps	

### Notes:

1. 
$$RL_{dc}(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.05 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases}$$

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Optical Data Rate per channel (PAM4)	DR		53.125		GBd	
Frequency Tracking	Ft	-100		100	ppm	
Center Wavelength	$\lambda_C$	844	850	863	nm	
RMS Spectral Width				0.6	nm	1
Laser Off Power	Poff			-30	dBm	
Average Optical Power	Pavg	-4.6		4	dBm	
Extinction Ratio	ER	2.5			dB	
Transmitter and Dispersion Eye Closure	TDECQ			4.4	dB	
Outer Optical Modulation Amplitude	OMAouter	-2.6		3.5	dBm	2
Encircled Flux, Each Lane		$\geq 86\% @ 19 \mu\text{m}$ $\leq 30\% @ 4.5 \mu\text{m}$			dB	3
Optical Return Loss Tolerance	ORLT			14	dB	
<b>Receiver</b>						
Electrical Data Rate Per Channel (PAM4)	DR		26.5625		GBd	
Frequency Tracking	Ft	-100		100	ppm	
Center Wavelength	$\lambda_r$	842	850	948	nm	
Damage Threshold		5			dBm	
Average Receive Power		-6.4		4	dBm	4
Receiver Reflectance				-15	dB	
Differential Data Output Voltage Peak to Peak Swing	Vopp	600		845	mV	
Receiver Sensitivity (OMAouter) (max) For $\text{TECQ} \leq 1.8\text{dB}$ For $1.8\text{dB} < \text{TECQ} \leq 4.4\text{dB}$	RS			-4.6 -6.4+TECQ	dBm dBm	
Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	

### Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ<1.8dB, the OMA (min) must exceed this value.
3. If measured into type A1a.2, type A1a.3 or type A1a.4, 50  $\mu\text{m}$  fiber, in accordance with IEC 61280-1-4.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.  
Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.6dB.

## Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTTL-I	ModSelL	Module Select	
9	LVTTTL-I	ResetL	Module Reset	
10		VccRx	3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2 Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2 Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3n	Transmitter Inverted Data Output	
15	CML-O	Rx3p	Transmitter Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1n	Transmitter Inverted Data Output	
18	CML-O	Rx1p	Transmitter Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Transmitter Inverted Data Output	
22	CML-O	Rx2p	Transmitter Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Transmitter Inverted Data Output	
25	CML-O	Rx4p	Transmitter Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTTL-O	ModPrsL	Module Present	
28	LVTTTL-O	IntL	Interrupt	
29		VccRx	3.3V Power Supply Transmitter	2
30		Vcc I	3.3V Power Supply	2
31	LVTTTL-I	InitMode	Initialization mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	
32		GND	Ground	1
33	CML-I	Tx1n	Transmitter Inverted Data Input	
34	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1n	Transmitter Inverted Data Input	

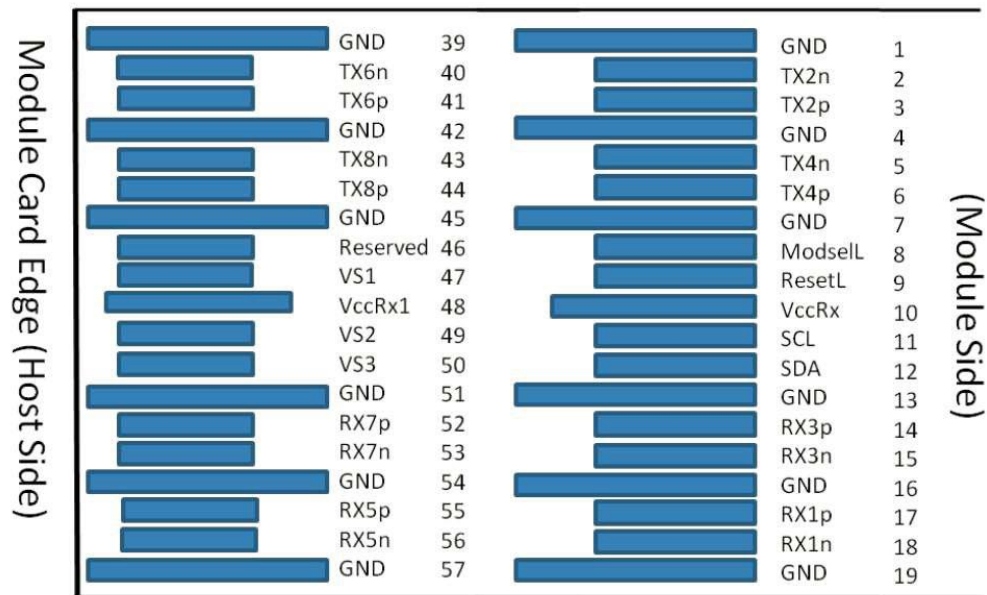
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	NC	3
47		VS1	NC	3
48		VccRx1	3.3V Power Supply	2
49		VS2	NC	3
50		VS3	NC	3
51		GND	Ground	1
52	CML-O	Rx7n	Transmitter Inverted Data Output	
53	CML-O	Rx7p	Transmitter Non-Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5n	Transmitter Inverted Data Output	
56	CML-O	Rx5p	Transmitter Non-Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Transmitter Inverted Data Output	
60	CML-O	Rx6p	Transmitter Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Transmitter Inverted Data Output	
63	CML-O	Rx8p	Transmitter Non-Inverted Data Output	
64		GND	Ground	1
65		NC	NC	3
66		Reserved	NC	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	NC	3
70		GND	Ground	1
71	CML-I	Tx7n	Transmitter Inverted Data Input	
72	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5n	Transmitter Inverted Data Input	
75	CML-I	Tx5p	Transmitter Non-Inverted Data Input	

76		GND	Ground	1
----	--	-----	--------	---

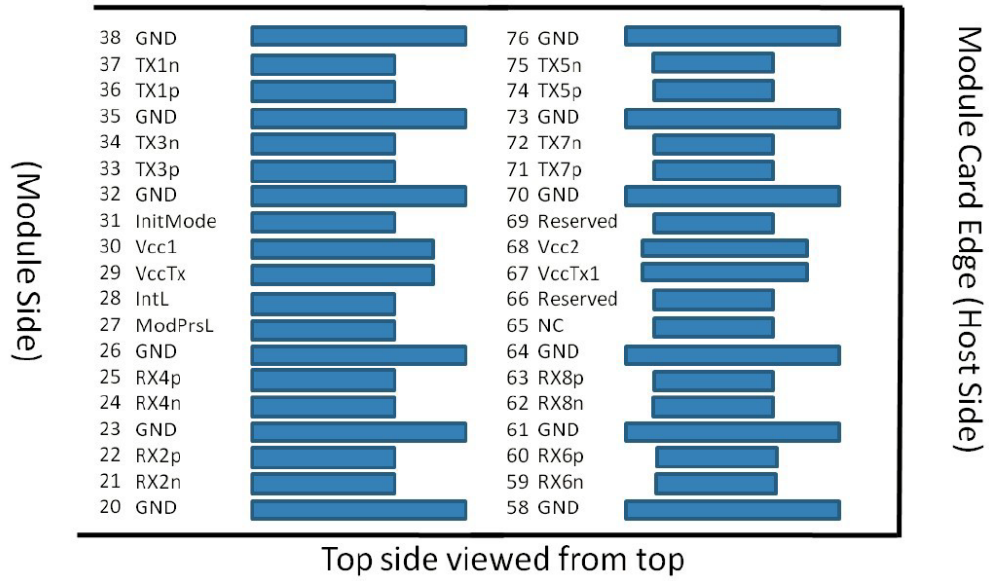
#### Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

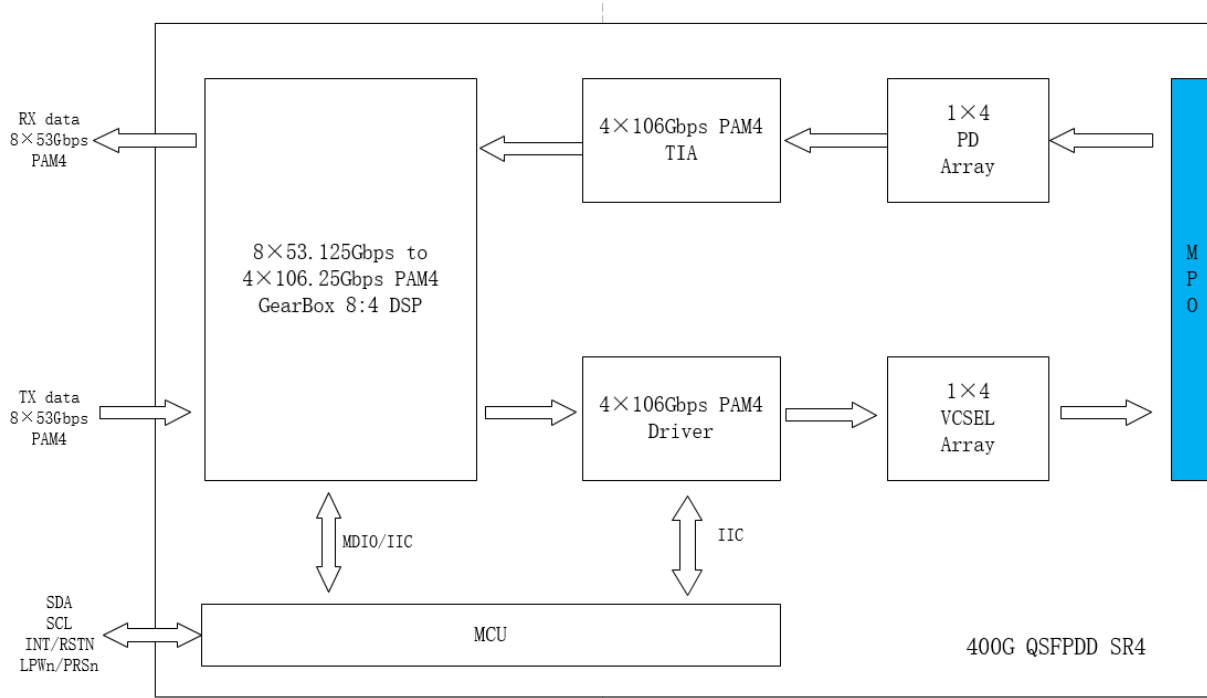
#### Electrical Pin-Out Details



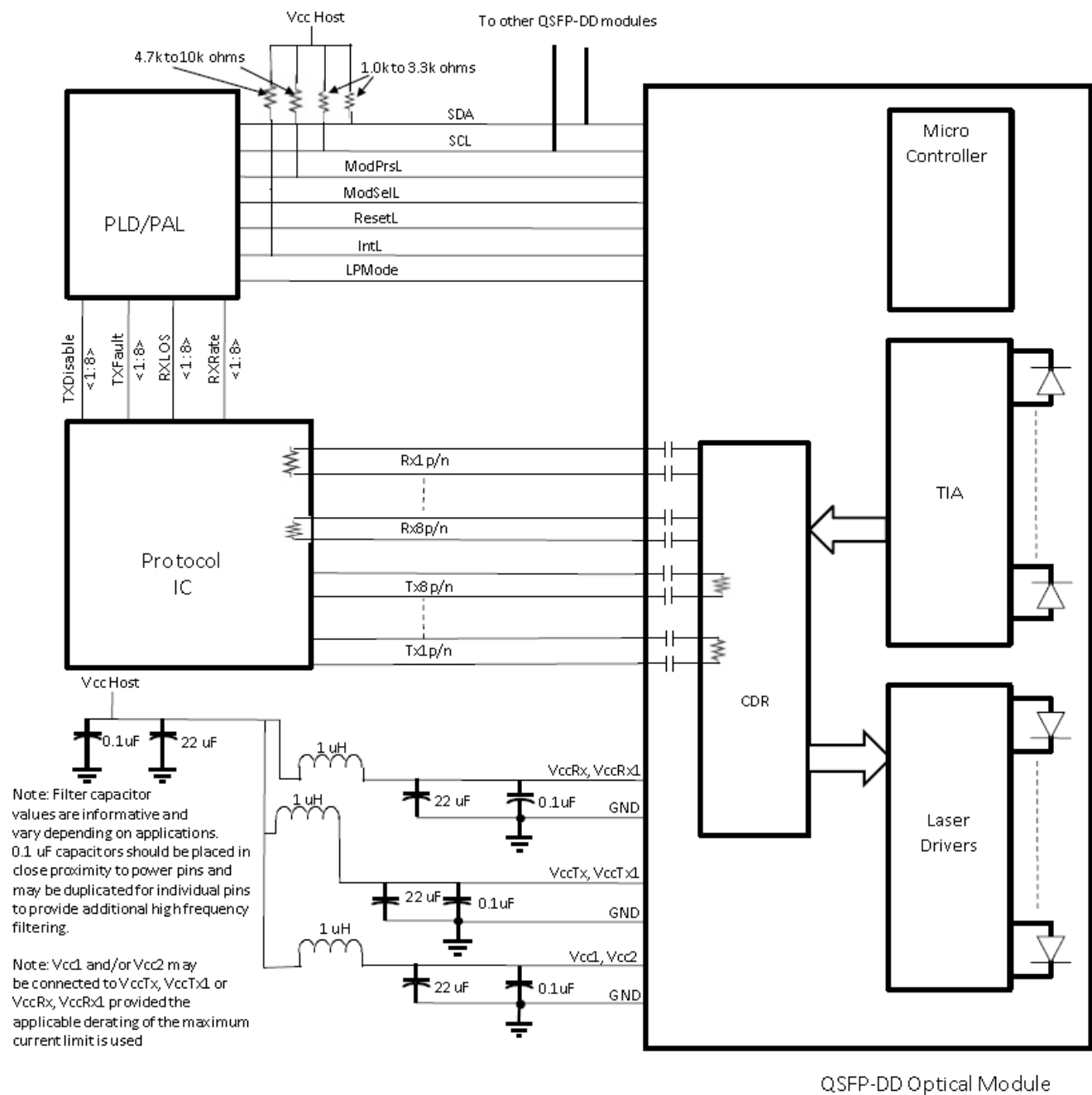
Bottom side viewed from bottom



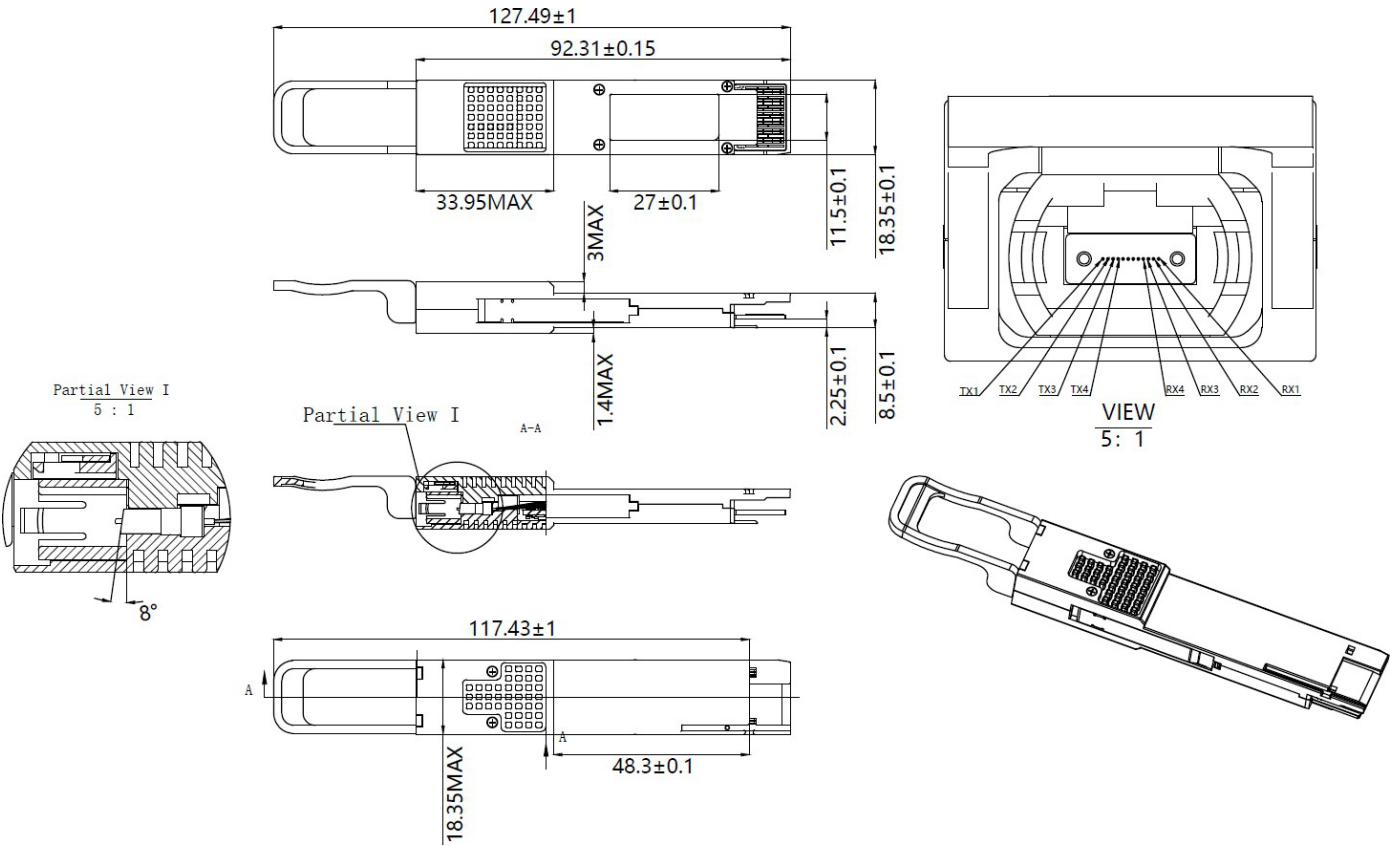
### Transceiver Block Diagram



Recommended Interface Circuit



**Mechanical Specifications**



## About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

## Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

## Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.



## Contact Information

ProLabs US

Email: [sales@prolabs.com](mailto:sales@prolabs.com)

Telephone: 952-852-0252

ProLabs UK

Email: [salesupport@prolabs.com](mailto:salesupport@prolabs.com)

Telephone: +44 1285 719 600