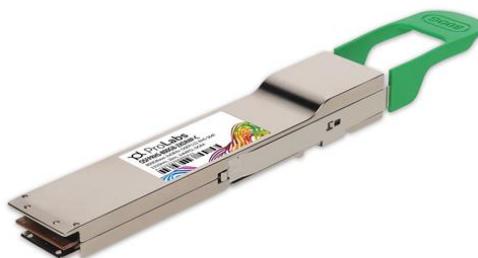


## OSFPRHS-800GB-2XDR4P-C

MSA and TAA 800GBase-2xDR4+ PAM4 OSFP112 RHS Transceiver (SMF, 1310nm, 2km, 2xMPO, DOM, CMIS 5.0)

### Features:

- Supports Both Ethernet and InfiniBand
- OSFP MSA Compliant
- Dual MPO-12 Connector APC
- Compliant with CMIS 5.0
- 8 Channels of 100G-PAM4 Electrical and Optical Parallel Lanes
- 2km Maximum Reach via Single-Mode Fiber
- Power Consumption: 14.5W
- Operating Temperature: 0 to 70 Celsius
- Class 1 Laser
- RoHS Compliant and Lead-Free



### Applications:

- 800GBase Ethernet

### Product Description

This MSA compliant OSFP112 RHS transceiver provides 800GBase-2xDR4+ throughput up to 2km over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")



## CMIS Application Advertisements

ApSEL Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 1	50 (400GAUI-4-L C2M)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1,5)
ApSel 2	32 (IB NDR)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1,5)
ApSel 3	F (200GAUI-4 C2M)	17 (200GBASE-DR4)	44 (4:4)	11 (lanes 1,5)
ApSel 4	31 (IB HDR)	17 (200GBASE-DR4)	44 (4:4)	11 (lanes 1,5)
ApSel 5	4C (100GAUI-1-L C2M)	14 (100GBASE-DR)	11 (1:1)	FF (lanes 1,2,3,4,5,6,7,8)
ApSel 6	52 (800GAUI-8-L C2M)	0 (Undefined)	88 (8:8)	01 (lane 1)
ApSel 7	4F (400GAUI-4-S C2M)	1C (400GBASE-DR4)	44 (4:4)	11 (lanes 1,5)
ApSel 8	4B (100GAUI-1-S C2M)	14 (100GBASE-DR)	11 (1:1)	FF (lanes 1,2,3,4,5,6,7,8)
ApSel 9	51 (800GAUI-8-S C2M)	0 (Undefined)	88 (8:8)	01 (lane 1)
ApSel 10	42 (CAUI-4 C2M with RS FEC)	F (100G PSM4 MSA)	44 (4:4)	11 (lanes 1,5)
ApSel 11	30 (IB EDR)	F (100G PSM4 MSA)	44 (4:4)	11 (lanes 1,5)

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Relative Humidity (Non-Condensing)	RH	0		85	%	
Data Rate Per Lane	DRL		53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10 <sup>-4</sup>		
Post-FEC Bit Error Ratio				1x10 <sup>-15</sup>		1
Link Distance	D	100		2000	m	2

### Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Power Supply Voltage</b>	Vcc	3.135	3.3	3.465	V	
<b>Power Consumption</b>				14.5	W	
<b>Module Input Per Lane</b>						
<b>Signaling Rate Per Lane</b>	TP1	$53.125 \pm 100\text{ppm}$			GBd	
<b>DC Common-Mode Input Voltage</b>	TP1	-0.35		2.85	V	
<b>Single-Ended Input Voltage</b>	TP1a	-0.4		3.3	V	
<b>AC Common-Mode RMS Input Voltage</b>	<b>Low-Frequency (VCMLF)</b>	TP1a	32		mV	
	<b>Full-Band (VCMFB)</b>		80			
<b>Module Stressed Input Test</b>		IEEE 802.3ck 120G3.4.3				
<b>Differential Peak-to-Peak Input Voltage Tolerance</b>	TP1a	750			mV	
<b>Common to Different Mode Input Return Loss</b>	TP1	IEEE 802.3ck Equation 120G-2				
<b>Effective Input Return Loss</b>	TP1	8.5			dB	
<b>Differential Input Termination Mismatch</b>	TP1			10	%	
<b>Module Output Per Lane</b>						
<b>Signaling Rate Per Lane</b>	TP4	$53.125 \pm 100\text{ppm}$			GBd	
<b>Differential Peak-to-Peak Output Voltage</b>	<b>Short-Mode</b>	TP4		600	mV	
	<b>Long-Mode</b>			845		
<b>AC Common-Mode Output Voltage, RMS</b>	<b>Low-Frequency (VCMLF)</b>	TP4		32	mV	
	<b>Full-Band (VCMFB)</b>			80		
<b>Differential Termination Mismatch</b>	TP4			10	%	
<b>Eye Height</b>	TP4	15			mV	
<b>Vertical Eye Closure (VEC)</b>	TP4			12	dB	
<b>Common-Mode to Differential-Mode Output Return Loss</b>	TP4	IEEE 802.3ck Equation 120G-1				dB
<b>Effective Return Loss</b>	TP4	8.5			dB	
<b>Output Transition Time (20-80%)</b>	TP4	8.5			ps	
<b>DC Common-Mode Output Voltage</b>	TP4	-350		2850	mV	
<b>Differential Termination Mismatch</b>	TP4			10	%	

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
<b>Center Wavelength</b>	$\lambda_C$	1304.5	1311	1317.5	nm	
<b>Data Rate Per Lane</b>		$53.125 \pm 100\text{ppm}$			GBd	
<b>Modulation Format</b>						
<b>Side-Mode Suppression Ratio</b>	SMSR	30			dB	
<b>Average Launch Power Per Lane</b>	Pavg	-3.1		4	dBm	1
<b>Outer Optical Modulation Amplitude (OMAouter) Per Lane</b>	Poma	Max. (-0.1-1.5+TDECQ)		4.2	dBm	2
<b>Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane</b>	TDECQ			3.4	dB	
<b>Transmitter Eye Closure for PAM4 (TECQ) Per Lane</b>	TECQ			3.4	dB	
<b>  TDECQ – TECQ  </b>				2.5	dB	
<b>Over-shoot/Under-shoot</b>				22	%	
<b>Transmitter Power Excursion</b>				2	dBm	
<b>Extinction Ratio</b>	ER	3.5			dB	
<b>RIN<sub>17.1</sub>OMA</b>	RIN			-136	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL			17.1	dB	
<b>Transmitter Reflectance</b>	TR			-26	dB	
<b>Transmitter Transition Time</b>	Tr			17	ps	
<b>Average Launch Power of Off Transmitter Per Lane</b>	Toff			-15	dBm	
<b>Receiver</b>						
<b>Center Wavelength</b>	$\lambda_C$	1304.5	1311	1317.5	nm	
<b>Data Rate Per Lane</b>		$53.125 \pm 100\text{ppm}$			GBd	
<b>Modulation Format</b>		PAM4				
<b>Damage Threshold Per Lane</b>	THd	5			dBm	3
<b>Average Receive Power Per Lane</b>	AOPR	-7.1		4	dBm	4
<b>Receive Power (OMAouter) Per Lane</b>				4.2	dBm	
<b>Receiver Sensitivity (OMAouter) Per Lane</b>	SEN			Equation 1	dBm	5
<b>Stressed Receiver Sensitivity (OMAouter) Per Lane</b>	SRS			-2.5	dBm	6
<b>Receiver Reflectance</b>	RR			-26	dB	
<b>LOS Assert</b>	LOSA	-15		-10.5	dBm	
<b>LOS De-Assert</b>	LOSD			-7.5	dBm	
<b>LOS Hysteresis</b>	LOSH	0.5			dBm	
<b>Conditions of Stress Receiver Sensitivity (Note 7)</b>						
<b>Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test</b>				3.4	dB	

**Notes:**

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for  $OMA_{outer}(\text{minimum})$  vary with TDECQ. The Illustration of Transmitter  $OMA_{outer}$  and Receiver Sensitivity Mask below illustrates this along with values for  $OMA_{outer}$  (maximum).
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulation optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receiver power, per lane(minimum), is informative and not the principle indicator of signal strength. A receiver power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity ( $OMA_{outer}$ ) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), illustrated in the Illustration of Transmitter  $OMA_{outer}$  and Receiver Sensitivity Mask below.

$$RS = \max. (-4.5, TECQ - 5.9) \text{ dBm}$$

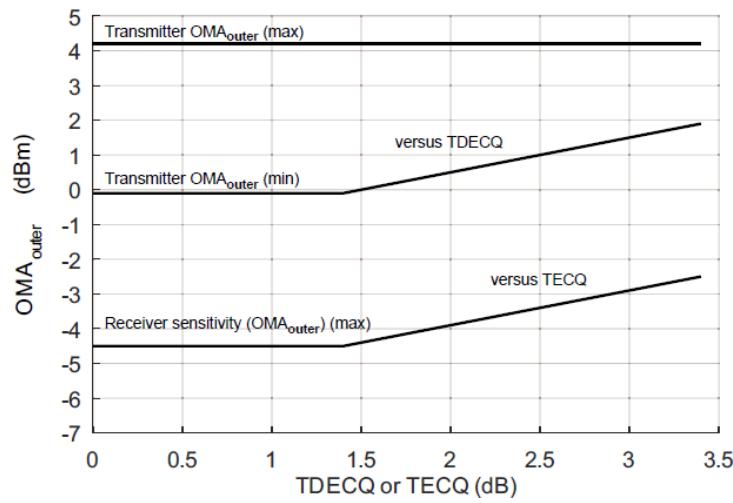
Where:

RS is the receiver sensitivity

TECQ is the TECQ of transmitter used to measure the receiver sensitivity

6. Measured with conformance test signal at TP3 for the  $BER = 2.4 \times 10^{-4}$ .
7. The test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

**Illustration of Transmitter  $OMA_{outer}$  and Receiver Sensitivity Mask**

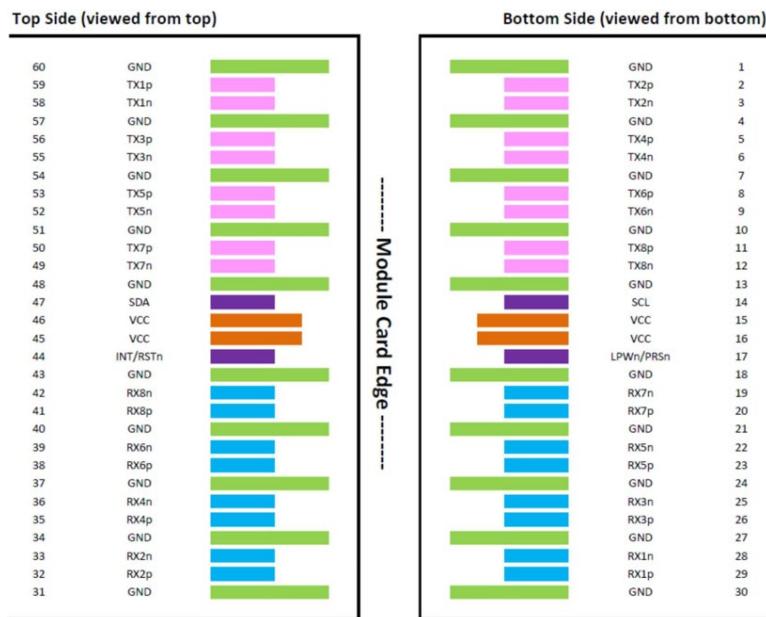


## Pin Descriptions

Pin	Logic	Symbol	Name/Description	Direction	Plug Sequence	Notes
1		GND	Module Ground.		1	
2	CML-I	Tx2+	Transmitter Data Non-Inverted.	Input from Host	3	
3	CML-I	Tx2-	Transmitter Data Inverted.	Input from Host	3	
4		GND	Module Ground.		1	
5	CML-I	Tx4+	Transmitter Data Non-Inverted.	Input from Host	3	
6	CML-I	Tx4-	Transmitter Data Inverted.	Input from Host	3	
7		GND	Module Ground.		1	
8	CML-I	Tx6+	Transmitter Data Non-Inverted.	Input from Host	3	
9	CML-I	Tx6-	Transmitter Data Inverted.	Input from Host	3	
10		GND	Module Ground.		1	
11	CML-I	Tx8+	Transmitter Data Non-Inverted.	Input from Host	3	
12	CML-I	Tx8-	Transmitter Data Inverted.	Input from Host	3	
13		GND	Module Ground.		1	
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	Bi-Directional	3	
15		Vcc	+3.3V Power.	Power from Host	2	
16		Vcc	+3.3V Power.	Power from Host	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	Bi-Directional	3	
18		GND	Module Ground.		1	
19	CML-O	Rx7-	Receiver Data Inverted.	Output to Host	3	
20	CML-O	Rx7+	Receiver Data Non-Inverted.	Output to Host	3	
21		GND	Module Ground.		1	
22	CML-O	Rx5-	Receiver Data Inverted.	Output to Host	3	
23	CML-O	Rx5+	Receiver Data Non-Inverted.	Output to Host	3	
24		GND	Module Ground.		1	
25	CML-O	Rx3-	Receiver Data Inverted.	Output to Host	3	
26	CML-O	Rx3+	Receiver Data Non-Inverted.	Output to Host	3	
27		GND	Module Ground.		1	
28	CML-O	Rx1-	Receiver Data Inverted.	Output to Host	3	
29	CML-O	Rx1+	Receiver Data Non-Inverted.	Output to Host	3	
30		GND	Module Ground.		1	
31		GND	Module Ground.		1	
32	CML-O	Rx2+	Receiver Data Non-Inverted.	Output to Host	3	
33	CML-O	Rx2-	Receiver Data Inverted.	Output to Host	3	
34		GND	Module Ground.		1	
35	CML-O	Rx4+	Receiver Data Non-Inverted.	Output to Host	3	
36	CML-O	Rx4-	Receiver Data Inverted.	Output to Host	3	
37		GND	Module Ground.		1	
38	CML-O	Rx6+	Receiver Data Non-Inverted.	Output to Host	3	
39	CML-O	Rx6-	Receiver Data Inverted.	Output to Host	3	

<b>40</b>		GND	Module Ground.		1	
<b>41</b>	CML-O	Rx8+	Receiver Data Non-Inverted.	Output to Host	3	
<b>42</b>	CML-O	Rx8-	Receiver Data Inverted.	Output to Host	3	
<b>43</b>		GND	Module Ground.		1	
<b>44</b>	Multi-Level	INT/RSTn	Module Interrupt/Module Reset.	Bi-Directional	3	
<b>45</b>		Vcc	+3.3V Power.	Power from Host	2	
<b>46</b>		Vcc	+3.3V Power.	Power from Host	2	
<b>47</b>	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	Bi-Directional	3	
<b>48</b>		GND	Module Ground.		1	
<b>49</b>	CML-I	Tx7-	Transmitter Data Inverted.	Input from Host	3	
<b>50</b>	CML-I	Tx7+	Transmitter Data Non-Inverted.	Input from Host	3	
<b>51</b>		GND	Module Ground.		1	
<b>52</b>	CML-I	Tx5-	Transmitter Data Inverted.	Input from Host	3	
<b>53</b>	CML-I	Tx5+	Transmitter Data Non-Inverted.	Input from Host	3	
<b>54</b>		GND	Module Ground.		1	
<b>55</b>	CML-I	Tx3-	Transmitter Data Inverted.	Input from Host	3	
<b>56</b>	CML-I	Tx3+	Transmitter Data Non-Inverted.	Input from Host	3	
<b>57</b>		GND	Module Ground.		1	
<b>58</b>	CML-I	Tx1-	Transmitter Data Inverted.	Input from Host	3	
<b>59</b>	CML-I	Tx1+	Transmitter Data Non-Inverted.	Input from Host	3	
<b>60</b>		GND	Module Ground.		1	

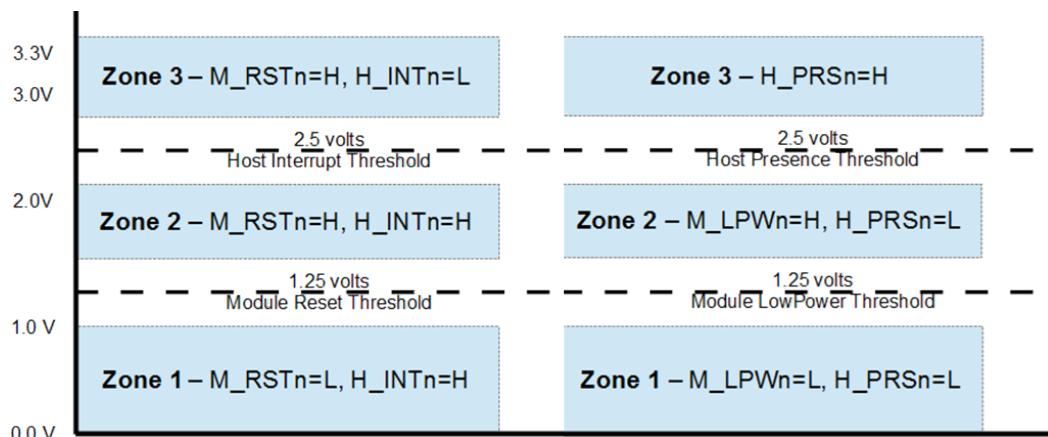
## Electrical Pad Layout



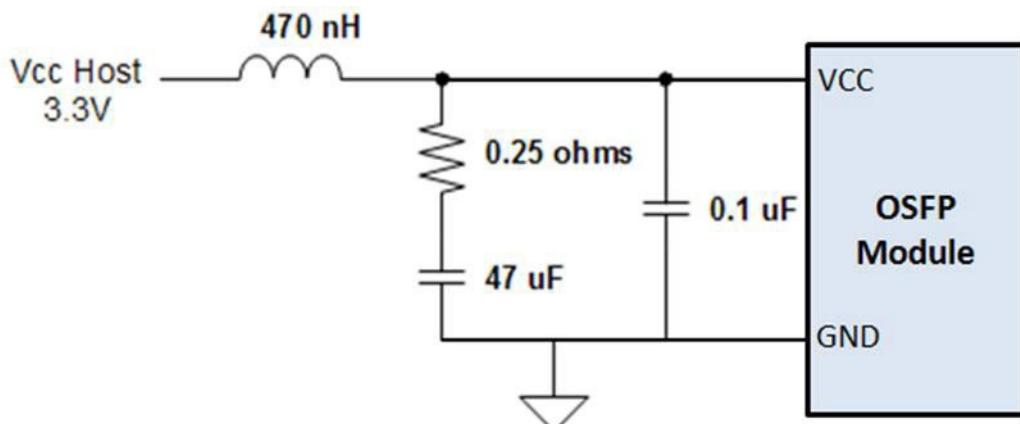
## OSFP Control Pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to +3.3V on host.
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to +3.3V on host.
LPWn/PRS <sub>n</sub>	Input/Output	<p>Dual Function Signal</p> <ul style="list-style-type: none"> <li>Low-Power Mode is an active-low input signal.</li> <li>Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal.</li> <li>Voltage zones is shown in the figure below.</li> </ul>
INT/RST <sub>n</sub>	Input/Output	<p>Dual Function Signal</p> <ul style="list-style-type: none"> <li>Reset is an active-low input signal.</li> <li>Interrupt is an active-high output signal voltage zones is shown in the figure below.</li> </ul>

## Voltage Zones



## Recommended Power Supply Filter

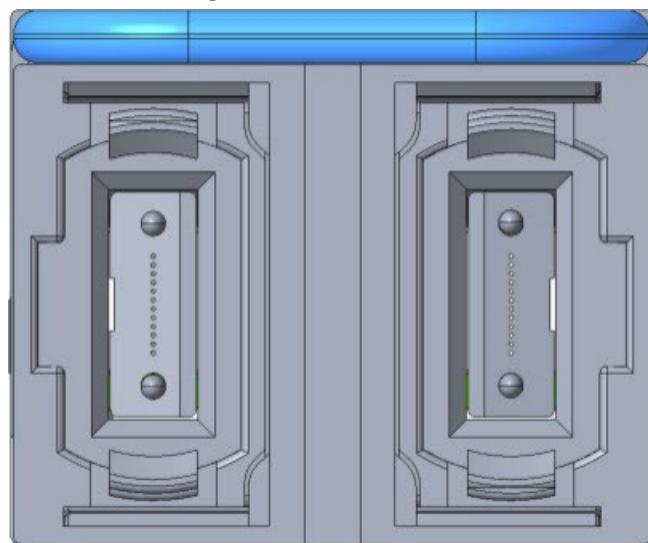


## Optical Port Descriptions

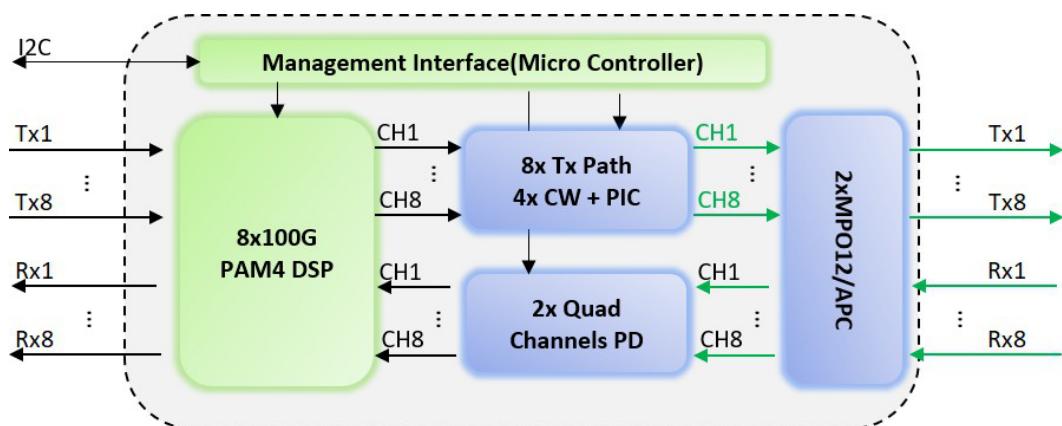
The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in the figure below when looking into the MDI receptacle with the connector keyway feature on top.

Aligned keys are used to ensure alignment between the modules and the patch cords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. **Note:** 2 alignment pins are present in each receptacle.

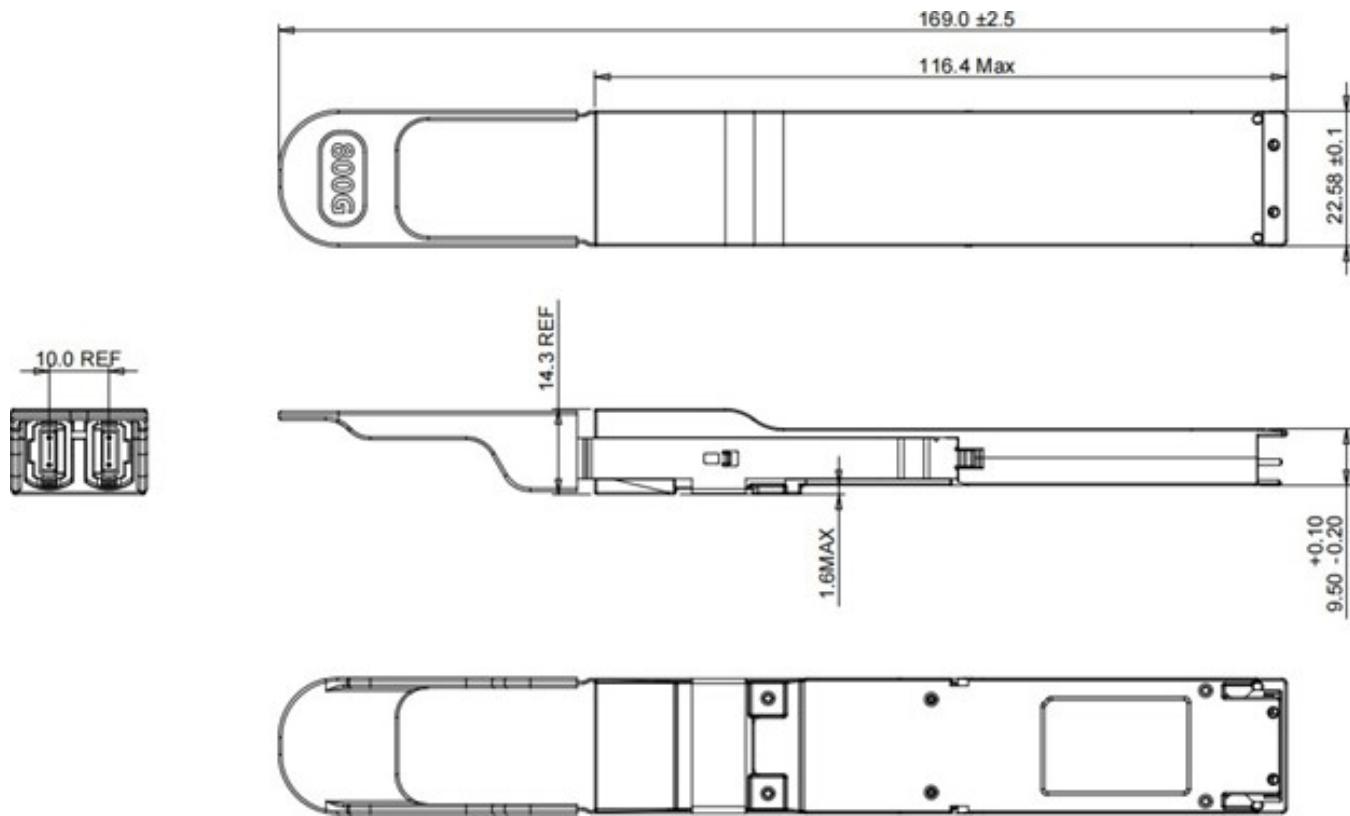
## Optical Media-Dependent Interface Port Assignments



## Transceiver Block Diagram



## Mechanical Specifications



## About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

## Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

## Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.



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